CLAIMS

Although Applicants have not amended the claims by the present Response, Applicants provide the following listing of the claims as a convenience to the Examiner.

Listing of the Claims

1-17. (canceled)

18. (withdrawn) A method for making a memory device, comprising the steps of:

providing a substrate having a first conductive line therein;

forming a plurality of diode access device memory cells in electrical communication with said first conductive line;

forming a second conductive line, said second conductive line in electrical communication with one of said memory cells; and

forming a third conductive line in electrical communication with said first conductive line and said plurality of memory cells.

19. (original) A method for making a memory device, comprising the steps of:

providing a substrate having a first conductive line therein;

forming a plurality of memory cells, each said memory cell comprising an element programmable to multiple states of resistance;

forming a second conductive line, said second conductive line in electrical communication with one of said memory cells; and

creating a third conductive line in electrical communication with said first conductive line and said plurality of memory cells.

20. (original) A method for forming a memory array, comprising the steps of:

forming a digit line in a substrate;

forming a plurality of memory cells in a first insulative layer, said memory cells overlying said digit line and in electrical communication with said digit line, each memory cell comprising an element having an alterable resistance, said first insulative layer having an opening therein;

forming a contact plug in said opening, said plug in electrical communication with said digit line;

forming a plurality of first conductive lines disposed with one of said first conductive lines overlying and in electrical communication with a selected one of said memory cells; and

forming a second conductive line in a second conductive layer, said second conductive line in electrical communication with said contact plug.

21. (original) A method of claim 20, wherein said step of forming said plurality of memory cells further comprises the steps of:

forming a plurality of diodes in said insulative layer, said diodes in electrical communication with said digit line; and

forming a plurality of programmable devices coupled with each of said diodes in electrical communication with a corresponding one of said elements of alterable resistance.

22 (withdrawn). The method, as set forth in claim 18, comprising the step of:

forming a plurality of contacts between the first conductive line and the third conductive line, a respective one of the plurality of contacts being formed between respective pairs of memory cells.

23 (withdrawn). The method, as set forth in claim 18, wherein the step of providing the first conductive line comprises the step of:

forming a titanium silicide layer over the first conductive line.

24 (withdrawn). The method, as set forth in claim 18, wherein the step of forming a plurality of diode access device memory cells comprises the steps of:

for each of the memory cells, forming an access device having a first terminal and a second terminal, the first terminal being in electrical communication with the first conductive line; and

for each of the memory cells, forming a memory element in electrical communication with the second terminal of the access device.

25 (withdrawn). The method, as set forth in claim 24, wherein the step of forming an access device comprises the step of:

forming a diode.

26 (withdrawn). The method, as set forth in claim 24, wherein the step of forming a memory element comprises the step of:

forming a chalcogenide memory element.

27 (withdrawn). The method, as set forth in claim 18, wherein the step of forming a plurality of diode access device memory cells comprises the step of:

forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit.

28 (withdrawn). The method, as set forth in claim 27, wherein the step of forming a plurality of diode access device memory cells comprises the step of:

forming pairs of memory cells, each pair being spaced apart by a distance approximately equal to the minimum photolithographic limit.

29 (withdrawn). The method, as set forth in claim 22, wherein the step of forming a plurality of contacts comprises the step of:

forming each contact from a doped semiconductive region of the substrate.

30 (withdrawn). The method, as set forth in claim 22, wherein the step of forming a plurality of contacts comprises the steps of:

forming dielectric spacers between each pair of memory cells; and

forming each contact between the respective dielectric spacers.

31 (withdrawn). The method, as set forth in claim 30, wherein each contact and its respective dielectric spacers have a combined width approximately equal to a minimum photolithographic limit.

32 (withdrawn). The method, as set forth in claim 22, wherein the step of forming a third conductive line comprises the step of:

isolating each of the plurality of memory cells from the plurality of contacts.

33 (withdrawn). The method, as set forth in claim 32, wherein the step of isolating comprises the step of:

disposing dielectric material on each of the plurality of memory cells.

34 (withdrawn). The method, as set forth in claim 33, wherein the step of forming the third conductive line comprises the step of:

forming the third line through tapered holes extending through the dielectric material to the contacts.

35 (previously presented). The method, as set forth in claim 19, comprising the step of:

forming a plurality of contacts between the first conductive line and the third conductive line, a respective one of the plurality of contacts being formed between respective pairs of memory cells.

36 (previously presented). The method, as set forth in claim 19, wherein the step of providing the first conductive line comprises the step of:

forming a titanium silicide layer over the first conductive line.

37 (withdrawn). The method, as set forth in claim 19, wherein the step of forming a plurality of memory cells comprises the steps of:

for each of the memory cells, forming an access device having a first terminal and a second terminal, the first terminal being in electrical communication with the first conductive line; and

for each of the memory cells, forming the element in electrical communication with the second terminal of the access device.

38 (withdrawn). The method, as set forth in claim 37, wherein the step of forming an access device comprises the step of:

forming a diode.

39 (previously presented). The method, as set forth in claim 37, wherein the step of forming the element comprises the step of:

forming a chalcogenide memory element.

40 (previously presented). The method, as set forth in claim 19, wherein the step of forming a plurality of memory cells comprises the step of:

forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit.

41 (previously presented). The method, as set forth in claim 40, wherein the step of forming a plurality of memory cells comprises the step of:

forming pairs of memory cells, each pair being spaced apart by a distance approximately equal to the minimum photolithographic limit.

42 (previously presented). The method, as set forth in claim 35, wherein the step of forming a plurality of contacts comprises the step of:

forming each contact from a doped semiconductive region of the substrate.

43 (previously presented). The method, as set forth in claim 35, wherein the step of forming a plurality of contacts comprises the steps of:

forming dielectric spacers between each pair of memory cells; and

forming each contact between the respective dielectric spacers.

44 (previously presented). The method, as set forth in claim 43, wherein each contact and its respective dielectric spacers have a combined width approximately equal to a minimum photolithographic limit.

45 (previously presented). The method, as set forth in claim 35, wherein the step of forming a third conductive line comprises the step of:

isolating each of the plurality of memory cells from the plurality of contacts.

46 (previously presented). The method, as set forth in claim 45, wherein the step of isolating comprises the step of:

disposing dielectric material on each of the plurality of memory cells.

47 (previously presented). The method, as set forth in claim 46, wherein the step of forming the third conductive line comprises the step of:

forming the third conductive line through tapered holes extending through the dielectric material to the contacts.

48 (previously presented). The method, as set forth in claim 20, comprising the step of:

forming a plurality of contact plugs between the digit line and the second conductive line, a respective one of the plurality of contact plugs being formed between respective pairs of memory cells.

49 (previously presented). The method, as set forth in claim 20, wherein the step of forming the digit line comprises the step of:

forming a titanium silicide layer over the digit line.

50 (withdrawn). The method, as set forth in claim 20, wherein the step of forming a plurality of memory cells comprises the steps of:

for each of the memory cells, forming an access device having a first terminal and a second terminal, the first terminal being in electrical communication with the digit line; and

for each of the memory cells, forming the element in electrical communication with the second terminal of the access device.

51 (withdrawn). The method, as set forth in claim 50, wherein the step of forming an access device comprises the step of:

forming a diode.

52 (previously presented). The method, as set forth in claim 50, wherein the step of forming the element comprises the step of:

forming a chalcogenide memory element.

53 (previously presented). The method, as set forth in claim 20, wherein the step of forming a plurality of memory cells comprises the step of:

forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit.

54 (previously presented). The method, as set forth in claim 20, wherein the step of forming a plurality of memory cells comprises the step of:

forming pairs of memory cells, each pair being spaced apart by a distance approximately equal to the minimum photolithographic limit.

55 (previously presented). The method, as set forth in claim 48, wherein the step of forming a plurality of contact plugs comprises the step of:

forming each contact plug from a doped semiconductive region of the substrate.

56 (previously presented). The method, as set forth in claim 48, wherein the step of forming a plurality of contact plugs comprises the steps of:

forming dielectric spacers between each pair of memory cells; and

forming each contact plug between the respective dielectric spacers.

57 (previously presented). The method, as set forth in claim 56, wherein each contact plug and its respective dielectric spacers have a combined width approximately equal to a minimum photolithographic limit.

58 (previously presented). The method, as set forth in claim 48, wherein the step of forming a second conductive line comprises the step of:

isolating each of the plurality of memory cells from the plurality of contact plugs.

59 (previously presented). The method, as set forth in claim 58, wherein the step of isolating comprises the step of:

disposing dielectric material on each of the plurality of memory cells.

60 (previously presented). The method, as set forth in claim 59, wherein the step of forming the second conductive line comprises the step of:

forming the second conductive line through tapered holes extending through the dielectric material to the contact plugs.